

# ML12054A 2.0 GHz Super Low Power Dual Modulus Prescaler

## MECL PLL COMPONENTS ÷64/65, ÷128/129 SEMICONDUCTOR TECHNICAL DATA

## Legacy Device: Motorola MC12054A

The ML12054A is a super low power dual modulus prescaler used in phase-locked loop applications with low power dissipation of 5.4 mW at a minimum supply voltage of 2.7 V.

The ML12054A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx or Lansdale's ML145xxx series in a PLL to provide tuning signals up to 2.0 GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0 GHz Toggle Frequency
- The ML12054A is Pin and Functionally Compatible with the Motorola MC12031
- Low Supply Current 2.0 mA Typical
- 2.6mA Maximum,  $V_{CC} = 2.7$  to 5.5 Vdc
- Short Setup Time (T<sub>set</sub>) 10ns Maximum @ 2.0 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Maximum Input Voltage Should Be Limited to 6.5 Vdc
- Operating Temperature Range  $T_A = -40$  to  $85^{\circ}C$

## FUNCTIONAL TABLE

SW	MC	Divide Ratio
Н	Н	64
н	L	65
L	н	128
L	L	129

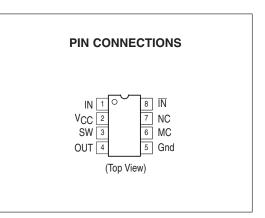
NOTES: 1. SW: H = V<sub>CC</sub>, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.

2. MC: H = 2.0 V to V<sub>CC</sub>, L = GND to 0.8 V.

### MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V <sub>CC</sub>	-0.5 to 7.0	Vdc
Operating Temperature Range	TA	-40 to 85	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to 150	°C
Modulus Control Input, Pin 6	MC	–0.5 to 6.5	Vdc

<b>SO 8 = -5P</b> PLASTIC PACKAGE CASE 751 1 (SO-8)							
PACKAGE	MOTOROLA	GINFORMATION LANSDALE					
SO 8	MC12054AD	ML12054A-5P					
<b>Note</b> : Lansdale lead free ( <b>Pb</b> ) product, as it becomes available, will be identified by a part number prefix change from <b>ML</b> to <b>MLE</b> .							

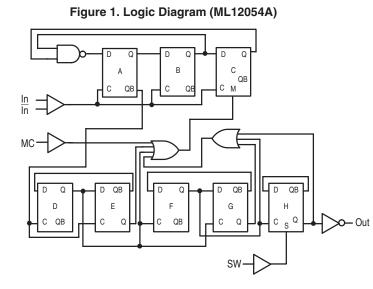


**ELECTRICAL CHARACTERISTICS** ( $V_{CC}$  = 2.7 to 5.5 Vdc,  $T_A$  = -40 to 85°C, unless otherwise noted.)

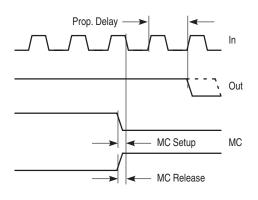
Characteristic	Symbol	Min	Тур	Мах	Unit
Toggle Frequency (Sine Wave Input)	ft	0.1	2.5	2.0	GHz
Supply Current (Pin 2)	ICC	-	2.0	2.6	mA
Modulus Control Input High (MC)	VIH1	2.0	-	V <sub>CC</sub> + 0.5 V	V
Modulus Control Input Low (MC)	VIL1	Gnd	-	0.8	V
Divide Ratio Control Input High (SW)	V <sub>IH2</sub>	$V_{CC} - 0.5 V$	VCC	V <sub>CC</sub> + 0.5 V	VDC
Divide Ratio Control Input Low (SW)	V <sub>IL2</sub>	Open	Open	Open	-
Output Voltage Swing (Note 2) (C <sub>L</sub> = 8.0 pF, R <sub>L</sub> = 1.65 k $\Omega$ )	Vout	0.8	1.1	-	V <sub>pp</sub>
Modulus Setup Time MC to Out @ 2000 MHz	t <sub>set</sub>	-	8.0	10	ns
Input Voltage Sensitivity 250–2000 MHz 100–250 MHz	V <sub>in</sub>	100 400		1000 1000	mVpp
Output Current (Note 1) $V_{CC} = 2.7$ V, C <sub>L</sub> = 8.0 pF, R <sub>L</sub> = 1.65 kΩ $V_{CC} = 5.0$ V, C <sub>L</sub> = 8.0 pF, R <sub>L</sub> = 3.6 kΩ	IO		1.0 1.0	4.0 4.0	mA

NOTES: 1. Divide ratio of ÷64/65 @ 2.0 GHz

2. Valid over voltage range 2.7 to 5.5 V; RL = 1.65 k $\Omega$  @ V\_{CC} = 2.7 V; RL = 3.6 k $\Omega$  @ V\_{CC} = 5.0 V

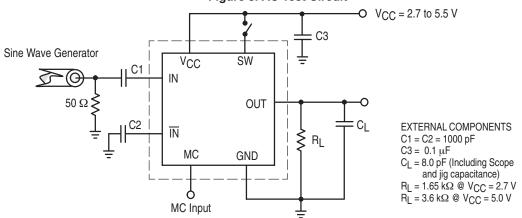


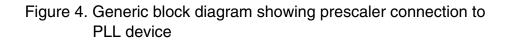
#### Figure 2. Modulus Setup Time



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.







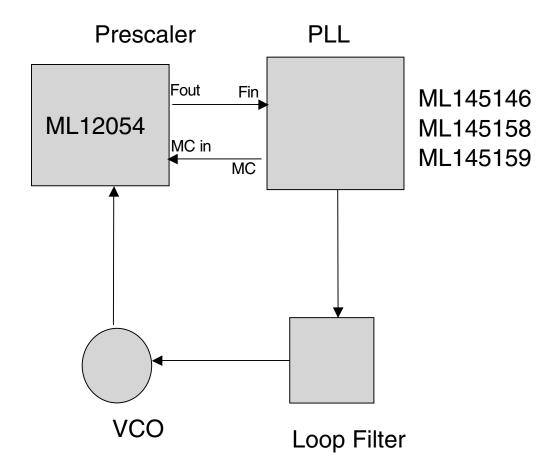
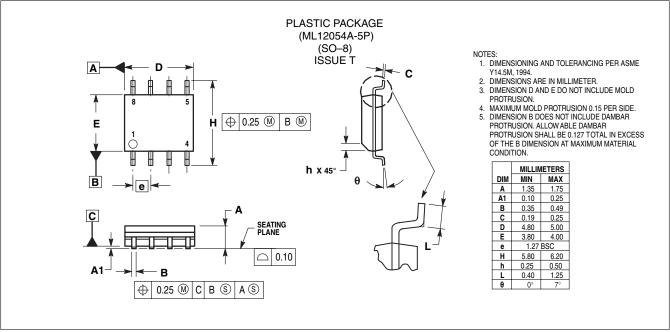


Figure 4 shows a generic block diagram for connecting a prescaler to a PLL device that supports dual modulus control. Application note AN535 decribes using a two-modulus prescaler technique.By using prescaler higher frequencies can be achieve than by a single CMOS PLL device.

#### **OUTLINE DIMENSIONS**



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